Combining Physical Test with Structural FEA to Develop Package-Specific Failure Models for Electronic Components

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1 Introduction

The use of electronics in harsh environments has increased significantly in the past few decades. For example, in automobiles, where electronic assemblies experience wide temperature extremes, temperature cycling, and shock, the cost of electronics was 18% of the total vehicle cost in the year 2000 and 40% of the total vehicle cost in 2020 [1]. Automotive electronic assemblies experience mechanical shock in a variety of scenarios such as a door slam, a vehicle crash or going over a pothole. In addition to the impact of component power dissipation on component temperatures, the automotive environment can include significant temperature variation due to diurnal solar loading, climate control, and engine heating/cooling cycles. The solder joints that connect electronic components to circuit boards are common failure locations in electronic assemblies, particularly in high shock/vibration environments and extreme temperature cycling conditions. Solder joint failure behavior is heavily influenced by the component's package construction and materials.

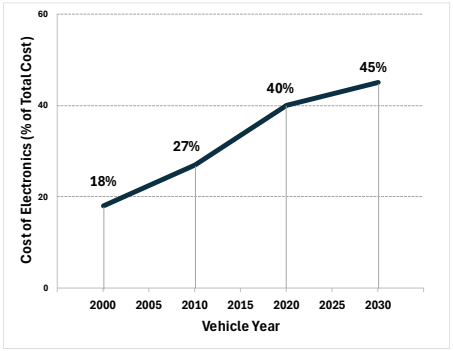

Fig. 1: Cost of Electronics in New Cars[1].

Qualification testing required to ensure that the component and system designs meet verification and validation requirements with respect to performance and manufacturing, can be expensive and time consuming. Using a finite element approach, component-level failure models can be used in conjunction with simulation to predict load-specific times to failure and virtually test designs to gain confidence ahead of physical qualification testing. Although many failure models exist for common failure mechanisms in electronics, they include parameters that need to be defined for the specific materials and assembly methods involved. Acquiring accurate material properties is often the biggest challenge to understanding component behavior under load and defining failure model parameters. While data sheets can be helpful, they typically only include some of the failure model parameters of interest and may be missing key material properties; especially if those properties vary over the range of environmental conditions of interest.

The methods discussed in this paper have been used to create and validate component-level failure models under thermal cycling and shock loads that can be used in system-level simulations of product designs. The approach leverages test and measurement to capture accurate dimensional and material property data as inputs for finite element component models and to help tune the component failure models based on component-level test results. It is not practical or necessary to apply this approach for every component on a printed circuit board assembly. For critical components, however, where component failure has a high impact on product reliability or safety, the approach can be very useful to better understand failure behavior.

2 Problem Definition and Approach

In early-stage product design, decisions concerning board layout, materials, and manufacturing methods for printed circuit board assemblies (PCBAs) are often undefined; making full-scale, high-fidelity simulations of PCBA reliability infeasible at this stage. In addition, waiting until these critical design decisions are made can jeopardize aggressive go to market timelines. The solution is to develop and validate models of component reliability that can be used to establish component-specific design limits and enable early-stage design studies. The Ansys Reliability Engineering Services team was

approached by a client who wanted to incorporate two new electronic components into a series of upcoming designs, in use environments where thermal cycling and mechanical shock were critical design loads.

2.1 Components of Interest

The two components of interest for the reliability analysis were packaged as ball grid arrays (BGAs) and were identified by the client as potential drivers of reliability, based on experience with similar electronic packages, products, and use environments. BGA packages are commonly used for complex integrated circuits to make hundreds or even thousands of input/output connections in the smallest footprint possible. The packages analyzed are typical of BGA construction and connect the active die circuitry to the PCB through wire bonds and solder balls (Fig. 2). The response of the package to thermal and mechanical loading is primarily a function of the effective coefficient of thermal expansion (CTE) and modulus, driven primarily by die dimensions and overmold and die attach material selection.

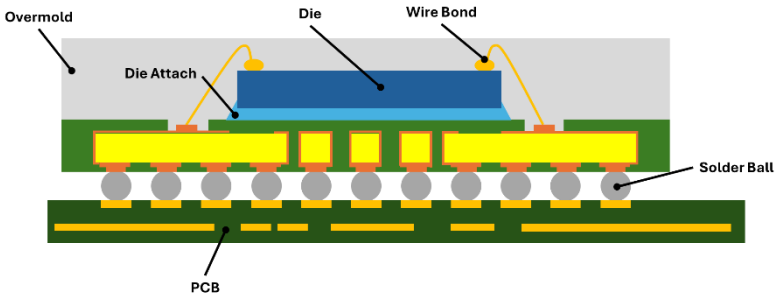

Fig. 2: Cross Section - Typical BGA Component Package and Attachment.

The primary failure mode of interest was fracture of the solder between the BGA component and the PCB. Under thermal cycling, the failure mechanism is solder fatigue, driven by CTE mismatch between the component and the PCB. Under shock loading, the fracture results from crack initiation and a series of crack extension events, driven by repetitive shock loads.

2.2 Failure Model Approaches

Failure modeling for solder joint fracture is a well-established field of study, with many different approaches proposed and tested over the last several decades[2]. Application areas include low cycle fatigue, high cycle fatigue, and thermal cycling with damage criteria such as plastic strain, total strain, accumulated strain energy, and strain energy density. Finding the appropriate approach for a given reliability problem depends on the application environment, component and board properties, the relevant loading scenarios, solder selection, and other factors. A full discussion of the different approaches is beyond the scope of this paper, but reference [2] is an excellent review for those interested. For the BGAs of interest in this study, an approach proposed by Syed was used for the thermal cycling load case[3] and Steinberg's work was used as the basis for the mechanical shock failure model[4].

2.2.1 Baseline Failure Models

Equation (1) illustrates the Syed approach where a power law relationship is used to estimate the number of thermal cycles to failure (N_f) for a solder joint, based on accumulated strain energy density or work (Δw) in each thermal cycle (where W' is the accumulated work at failure). The accumulated work per cycle is the damage metric in this approach and is typically calculated through finite element analysis (FEA) of the solder joints using a viscoplastic material model under thermal cycling loads. The work per cycle is extracted from the component side of the solder ball, in the region of highest strain (Fig. 3).

$$N_f = (W' \times \Delta w)^{-1} \quad (1)$$

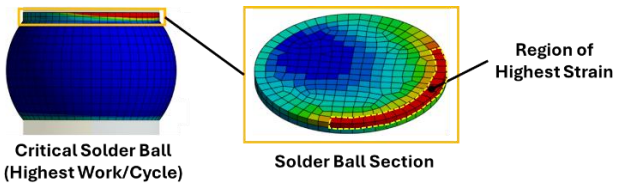

Fig. 3: Determination of work per cycle from finite element analysis.

Equation (2) illustrates the Steinberg approach which establishes a limit for PCB displacement ($Z_{3\sigma\ limit}$) as the damage metric, based on component geometry and placement, PCB thickness, and component type.

$$Z_{3\sigma\ limit} = \frac{0.00022B}{ChR\sqrt{L}} \quad (2)$$

Where,
$Z_{3\sigma}$ = single amplitude displacement limit to achieve solder fatigue life of 20 x 10^6 cycles
B = length of PCB edge parallel to component
C = constant based on the component package type
h = PCB thickness
R = relative position factor for the component on the PCB
L = length of the electronic component

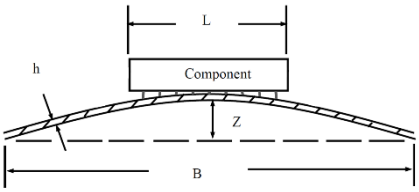

Fig. 4: Steinberg model parameters

2.2.2 Tailoring Models to the Components of Interest

The baseline failure models from literature often have suggested values for model constants, derived from FEA, testing, or both. In cases where the materials, component types and loading conditions are similar to those proposed in literature, the baseline models and constants can provide useful results. As component packaging and material technologies have progressed, however, it becomes more challenging to apply the baseline models as originally published. This is especially true for BGAs where the internal construction and bulk material properties can vary widely from component to component, affecting the CTE and modulus of the component. Table 1 summarizes some of the common variations in BGA construction that can impact the effective mechanical behavior of the component under thermal cycling and mechanical shock loading.

Component Feature	Common Variations
Substrate	Coreless substrates are typically the most compliant choices with the highest CTE. Organic substrates (i.e., epoxy and glass fiber) are stiffer and have a lower CTE (due to the glass content). Ceramic and silicon substrates have the highest modulus and lowest CTE.
Overmold	There is a large variation in modulus and CTE, even for plastic-overmolded BGAs, depending on the polymer material and the percent of fill material (typically glass). Bare-die designs do not use overmold at all, while others may include a metal lid with or without an overmold.
Die Dimensions	The die is one of the highest modulus, lowest CTE parts of a typical BGA. The thicker the die and the larger the area of the die, the more it can impact the effective CTE and modulus of the component. While Fig. 2 shows a single die, modern BGA components can have multiple die in stacked and other configurations.
Die Attachment	The example shown in Fig. 2 is of a wire-bonded die, attached to the substrate with a die attach material. BGAs in this configuration use widely different die attach materials, with varying modulus and CTE. Other BGA configurations eliminate the wire bonds entirely (e.g., a flip-chip) and attach the die to the substrate with solder.

Table 1. Common variations in BGA component construction.

2.3 Approach Summary

In early-stage product design, engineers need a way to estimate component-level solder joint reliability, pre-layout, to assess the suitability of the components for specific applications and make initial design decisions. The study detailed here focuses on two components where thermal cycling and mechanical shock are critical load cases across multiple product applications. By characterizing the mechanical properties of the components and conducting a series of thermal cycling and mechanical shock tests, Ansys was able to develop and validate component-level failure models that can be used to predict component reliability in a wide range of product applications.

3 Component Characterization

Prior to setting up the finite element models for the components of interest, it was critical to understand the relevant geometry and material properties. While follow-on testing would be used to confirm the mechanical behavior of the components, getting the finite element model to reflect that same behavior requires accurate dimensions and material properties. The two components of interest were a flash memory chip and a DDR memory chip. Fig. 5 shows the underside of each component (including the solder balls), and a component cross-section illustrating the basic internal configuration (b). Both components included a single wire bonded die, bonded to the substrate with a die attach material.

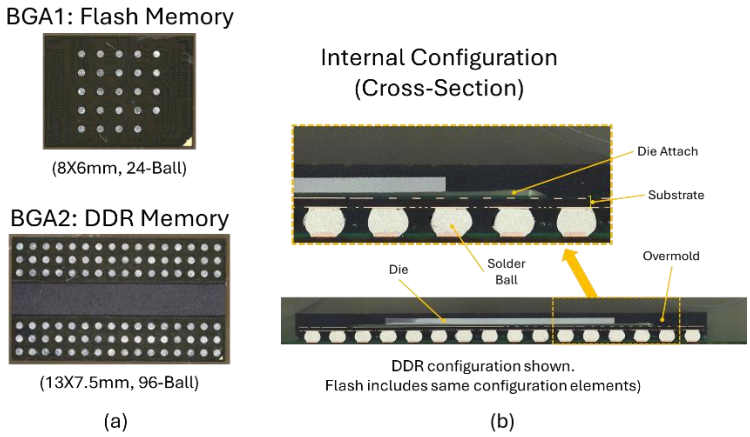

Fig. 5: Components configuration, (a) Components of interest;

(b) Baseline internal configuration (wire bonds not shown).

The component characterization process focused on verifying the construction of the component, critical dimensions, and the overall CTE of the package to ensure accurate inputs for finite element modeling. Initial examination of the components included optical microscopy and x-ray prior to destructive analysis. The packages were examined and measured under optical microscope to verify the data sheet dimensions and appearance. X-ray analysis was used to verify overall internal construction and help plan the destructive cross-sectional analysis.

The primary purpose of cross-sectional analysis was to verify the dimensions and location of structures internal to the component. Cross-sections parallel to the edges of the component exposed the die for measurement of thickness, length, width, and position of the die relative to the edges of the package. In addition, the cross-sections allowed measurement of the thickness of the substrate and the die attach material between the die and substrate. Fig. 6 shows example images from the construction and dimensional analyses.

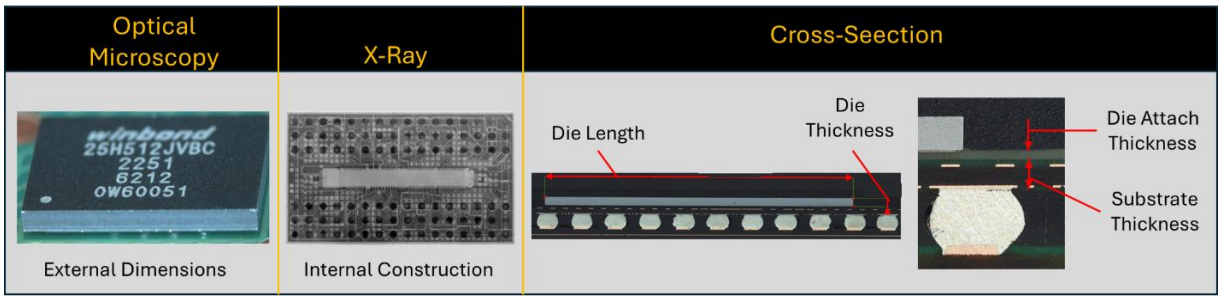

Fig. 6: Component Construction and Dimensional Analysis.

In addition to the construction and dimensional details, component characterization requires measurement of the effective in-plane CTE of the package. CTE mismatch between the PCB and component is typically the main driver of solder joint damage during thermal cycling. The mismatched expansion and contraction produced shear strain in the solder joints, leading to crack initiation and growth. Rather than measure the CTE for each material used in the construction of the component and

calculate an effective CTE using a rule-of-mixtures approach, a more practical and accurate approach is to measure package CTE directly using digital image correlation (DIC).

Digital image correlation is a non-contact full field optical technique that measures surface displacement under load. The technique is often used to measure displacement of tensile specimens, but can also be used for samples undergoing thermal cycling to measure displacement due to thermal expansion and contraction.

The components of interest for this study were prepared for DIC analysis and placed in a thermal chamber. Cameras on the exterior of the chamber were used to capture a series of component images as the chamber temperature was ramped from -55°C to 150°C. Post-processing of the image data for displacement versus temperature resulted in the strain data plotted in Fig. 7. The slope of a linear fit to the scatter-plot data is the effective component CTE. The effective CTE of the flash component was 7.8 parts-per-million/°C (PPM/°C). The effective CTE for the DDR component was 16.7 PPM/°C. The large difference in CTE between the two components illustrates the impact of die size on effective CTE. The area of the die in the flash component (light gray area in Fig. 7 planar cross-section) is very large compared to the area of the overmold (dark gray area in Fig. 7 planar cross-section). The die area in the DDR component, however, is much smaller compared to package size. The CTE of a typical silicon die material is in the 2-3 PPM/°C range, while epoxy overmold compounds typically range from 8-15 PPM/°C, depending on the amount of fill material used. With the die dominating the in-plane area of the flash component, the effective CTE of the component is driven more by the CTE of the die than the CTE of the overmold compound.

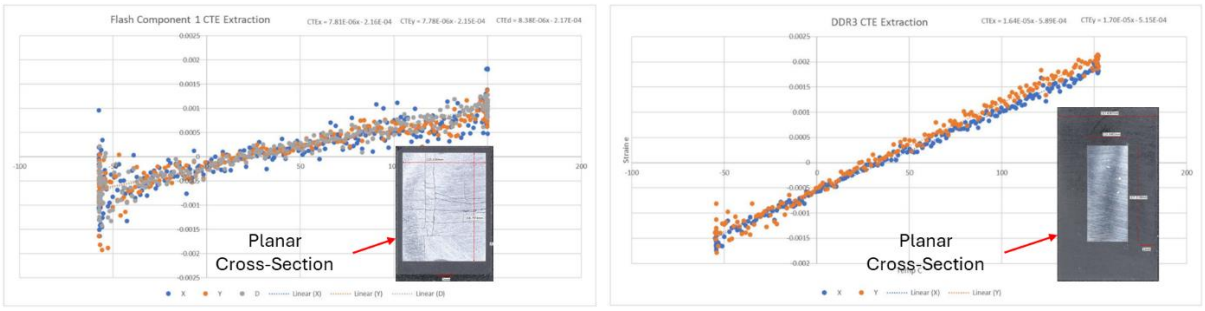

Fig. 7: CTE Measurement Data, (a) Flash component data and planar cross-section; (b) DDR component data and planar cross-section

The measured dimensions were used directly in the finite element models of the components. There is no direct input, however, for the effective CTE of the component. Matching CTE behavior between measurement and the FEA model required tuning of material properties within typical ranges, primarily for the substrate and overmold. While the die and die attach will have some effect on effective component CTE, the range of possible CTE values is much smaller for these materials.

4 Failure Model Development

The approach to failure model development combined component testing under thermal cycling and shock, along with simulation of the test conditions on a finite element model of each component. Test results were used to assess the time to failure. The finite element models were used to identify locations of maximum strain or calculate strain energy dissipation. Component testing and FEA results were used to define parameters for the appropriate baseline component-specific failure models.

4.1 Component Test Boards

Component testing required two different test board designs for each component; one for thermal cycle testing, the other for mechanical shock testing. The thermal cycling boards included 16 daisy-chained components in a 4 x 4 configuration, as shown in Fig. 8(a). The mechanical shock boards included a single daisy-chained component per board, as shown in Fig. 8(b). Daisy chaining is a method of linking selected solder joints in an electrical circuit. During testing, the resistance of the daisy chained circuits is continuously monitored. With all solder joints connected (i.e., no fractures), the resistance of the daisy chain is very low. When a solder joint in the chain fractures, it creates an open or partial-open in the

circuit that spikes the resistance, indicating the failure. The daisy-chained design of the test boards allowed accurate determination of time to failure in thermal cycling and mechanical shock tests.

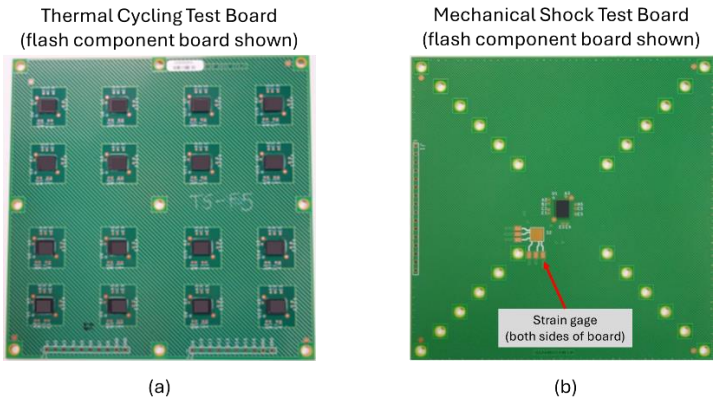

Fig. 8: Test Board Layout, (a) Thermal cycling test board; (b) Mechanical shock test board.

Each mechanical shock test board included a triaxial strain gage on both sides of the board, near the corner of the component. The strain gages captured the board strain profile during the shock pulse and the data were used to verify board strain predicted by the finite element model in the same region of the board.

4.2 Thermal Cycling

Thirty-two components of each component type were cycled between -55°C and 115°C, with 15-minute dwell times at the high and low temperature. Component failure was defined as at least one solder joint fracture, indicated by a spike in the resistance of the of the associated daisy-chained circuit. The test ran for just under 2400 cycles to achieve at least 40% failure of the population of components. 42% of the DDR components and 97% of the flash components had failed at test completion. Post-test cross-sectioning and optical microscopy inspection confirmed solder joint cracks at all failure sites indicated based on daisy-chain resistance measurements.

4.2.1 Test Results

Weibull analysis[6] of the time-to-failure data (Fig. 9) was performed to estimate the characteristic life for each component. Using a 2-parameter Weibull distribution, the β values (i.e. slope of the fit) for the flash and DDR failure data were both greater than 1, consistent with a wearout failure mechanism like solder fatigue. The η value for the Weibull fit is the characteristic life under thermal cycling, where characteristic life is the number of cycles at which 63.2% of the population is predicted to fail. In addition to the failure data, Fig. 9 includes cross-section images showing representative solder joint fractures for each component type.

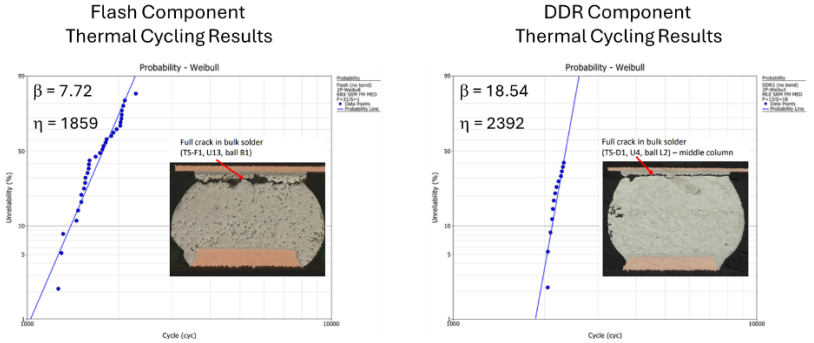

Fig. 9: Weibull analysis of thermal cycling time-to-failure data.

The characteristic life results reinforced the reason for pursuing testing and component-specific failure models. If the modulus and effective CTE of both components were assumed to be similar, the expectation would be that the larger component fails before the smaller component due to the larger

differential displacement per degree (between the PCB and the component) for the larger component. Larger differential displacement per degree results in a higher strain energy dissipation per cycle and shorter time to failure. Test results clearly show, however, that the smaller component (i.e., the flash component) fails in almost 25% fewer cycles than the larger component (i.e., the DDR component). Recall that the CTE of the flash component is less than half of the CTE for the DDR component (primarily due to the larger percentage of die area) and the similarity assumption breaks down, supporting the need for a component-specific failure model.

4.2.2 Thermal Cycling Models

Validation of the FEA model began with comparison of the known failure site in test to the region of maximum strain energy density in the model. All failures for the flash component occurred in a corner solder ball, at the ball-to-component connection. Fig. 10 shows a typical solder crack observed in test, along with the location of highest inelastic strain energy density in the FEA model. The observed failure site and the critical solder ball indicated by the FEA model correlated exactly, including the location of the failure site on the component side of the solder ball.

The failure sites for the DDR component occurred in solder balls near the corner of the die, rather than the corner of the component, on the component side of the solder ball. The FEA model showed the highest inelastic strain energy density at the same location (see Fig. 10). With a much lower percentage of die area in the DDR component, warping of the component during temperature cycling is more pronounced and adds a tensile component to the dominant shear strain due to CTE mismatch. The more complex state of solder joint strain in the DDR component makes the ball location of the failure site slightly more variable than for the flash component.

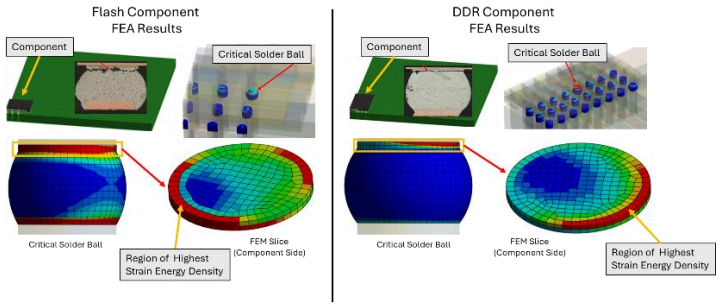

Fig. 10: Quarter-symmetric component FEA models (thermal cycling results).

Rearranging the Syed relationship in equation (1), allows estimation of the accumulated work at failure (W') for each component. The work per cycle (Δw) is derived from a volumetric average of creep strain energy density at the validated failure site in the FEA model. Table 2 summarizes the failure model parameters for both components.

$$W' = \frac{1}{N_f \Delta w} \tag{3}$$

Component	Characteristic Life (from test)	Δw (from FEA)	W'
Flash	1859 cycles	0.3177	0.0017
DDR	2392 cycles	0.0896	0.0047

Table 2: Thermal cycling failure model parameters.

4.3 Mechanical Shock

Five 5 components of each component type were exposed to a series of mechanical shocks, using a drop tower. Each shock was a 2500G half-sine pulse, 0.5 milliseconds in duration. A maximum of 31 drops was planned for each component to provide sufficient failure data for the modeling effort. Component failure was defined as at least one solder joint fracture, indicated by a spike in the resistance of the of the associated daisy-chained circuit. Due to the short duration of the drop event, a high-speed data acquisition system was used to sample daisy chain resistance and strain from the two strain gages

on each board at 200x10^3 samples/sec. Post-test cross-sectioning and optical microscopy inspection confirmed damage at all failure sites suspected based on daisy-chain resistance measurements.

4.3.1 Test Results

None of the flash components failed within 31 drops. There were no failure indications in the monitored daisy chain resistance data during test or signs of failure in the post-test cross-sectioning and optical inspection. One flash component was taken to failure, requiring 84 drops. The strain gages on the flash component test boards measured a maximum board strain of 2100 με.

All DDR components showed indications of daisy chain resistance spikes prior to 31 drops. Post-test cross-sectioning and optical inspection confirmed all failures, showing a combination of pad cratering, trace cracks, and solder fractures. The strain gages on the DDR component test boards measured a maximum board strain of 2200 με.

Weibull analysis of the time to failure data was conducted to estimate a characteristic life in terms of drops to failure. In the case of the flash component, where no failures were observed in test, a one parameter Weibull estimate[7], with β = 2.0 (assumes a combination of cumulative overstress and random failure mechanisms at play), resulted in a characteristic life of 83 drops to failure. For the DDR component case, the 2-parameter Weibull estimate yielded a characteristic life of 13 drops to failure.

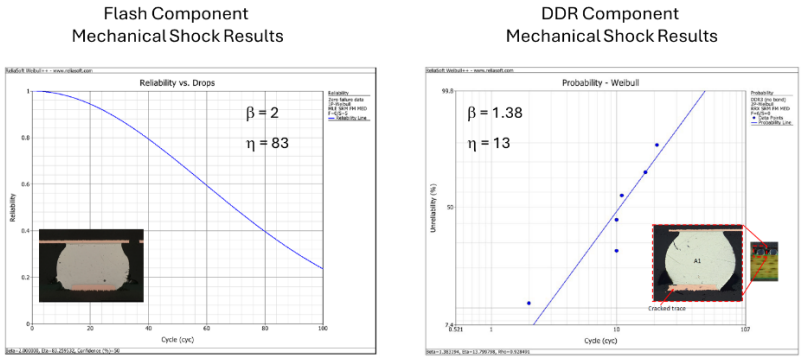

Figure 11: Mechanical shock time-to-failure data

4.3.2 Mechanical Shock Models

While the thermal cycling FEA models applied implicit solve techniques, the mechanical shock models used the LS-Dyna explicit solver due to the high strain rates involved. In addition, the mechanical shock models used 1D beam and 2D shell elements to model the solder balls (patch and beam technique) to minimize small elements and optimize run times for the explicit solve. The patch elements are linear elastic, while the beam elements (representing the solder) apply a multilinear isotropic hardening material model. The patch and beam approach was validated against a detailed model, using 3D elements for the solder ball mesh. Fig. 12 illustrates the different modeling approaches and shows a comparison of solder ball stress results between the different approaches.

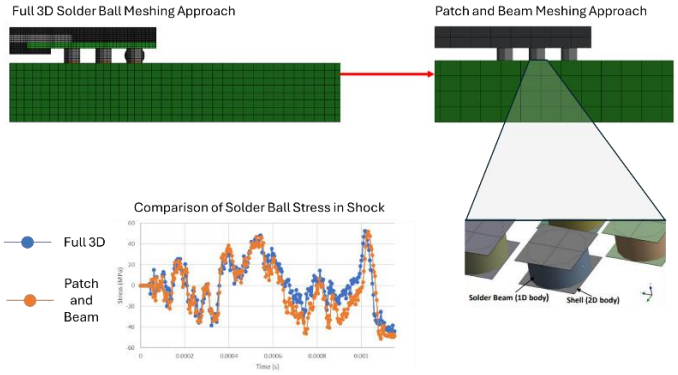

Fig. 12: Reduced order modeling technique for explicit analysis.

The strain data from the tri-axial strain gages near the corner of the component were used to validate finite element model predictions under the shock load experienced in test.

Rather than predicting cycles to failure, the focus of the mechanical shock failure modeling effort was to define a peak board strain near the component that could be used as a design limit when the flash or DDR components are incorporated into a product design. Given that the flash component performed well under the relatively aggressive test load (no failures out to 31 drops, with a characteristic life of 83 drops to failure), it was used as a baseline for determining peak board strain. The FEA model was used to calculate the peak board strain near the corner of the flash component during a 2500G half-sine, 0.5 millisecond shock event, resulting in a peak value of 2600 με. This was used as a conservative estimate of the peak board strain limit for the flash component.

The peak board strain limit for the DDR component was determined by using the length of the package diagonal to scale the peak strain for the flash component using the Steinberg relationship (equation (2)). Assuming a linear relationship between the Steinberg board displacement and board strain (valid for small displacements), the peak board strain (ε_{peak}) is used as the damage metric and is proportional to the board displacement limit ($Z_{3\sigma\ limit}$) (equation (4)).

$$\varepsilon_{peak} \propto \frac{0.00022B}{ChR\sqrt{L}} \tag{4}$$

Since the board thickness, board length, board width, component package type, and component placement are the same for the flash and the DDR components, the modified Steinberg relationship can be used to relate peak board strain based on package diagonal length (L) as shown in equation (5). Table 3 summarizes the peak board strain limits.

$$\left(\varepsilon_{peak\_DDR}\right)\sqrt{L_{DDR}} = \left(\varepsilon_{peak\_flash}\right)\sqrt{L_{flash}} \quad \rightarrow \quad \left(\varepsilon_{peak\_DDR}\right) = \left(\varepsilon_{peak\_flash}\right)\frac{\sqrt{L_{flash}}}{\sqrt{L_{DDR}}} \tag{5}$$

Component	Package Diagonal (mm)	Board Strain Limit (με)
Flash	10	2600 (from FEA)
DDR	15	2123 (from (5))

Table 3: Mechanical shock design limits.

Simulating the 2500G half-sine, 0.5 millisecond shock event on the DDR board, the peak strain in the critical area near the component corner was 2500 με, approximately 18% above the design limit. At this strain level, test results showed failure of all DDR components before reaching the maximum number of test drops, indicating progressive damage beyond the design limit.

5 Summary

Analytical methods and engineering simulation tools have been used for decades to predict component-level reliability of PCBA solder interconnects. The analytical methods are extremely efficient computationally and useful for many component types, under many real-world loading conditions. The limitation with these methods is that they make underlying assumptions about component design, component mechanical behavior, solder materials, and other factors that do not hold for many modern package designs and assembly methods. Detailed simulation of each component on the PCBA is one solution, assuming you have high confidence in material properties and dimensions, but that approach quickly becomes impractical for PCBAs with hundreds or thousands of individual components. This paper highlights an alternative approach where analytical methods can be used when assumptions hold, and simulation, in combination with component-level testing is used to better characterize interconnect reliability for more complex component packages.

6 Literature

References should be given in the last paragraph of your manuscript. Please use following scheme:

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